Monoimmittance logic R-elements

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Abstract—The general principles of monoimmittance logic elements and the design of schemes monoimmittance logic elements using the resistance to implement logic functions “NOT”, “AND” and “OR” are presented in the given article.

Keywords—logic elements; immitance; immitance logic level.

INTRODUCTION

Modern computer devices use video pulse signals for transferring and information processing [1, 2]. Simultaneously, optical [3], radio-frequency [4] and other signals find application for transferring and information processing but in much smaller degree. In these specific cases the choice of kind of signal is defined either the physical nature of the processed parameter, or improvement of information system parameters that can be achieved, for example, the possibility of processing of the information on carrier frequency of a signal, without its transformation to video pulse signals. Such problems can be solved with using of immitance logic elements [4]. As a information parameter in immitance logic elements uses combinations of resistive, inductive and capacitor immitance and it is possible to consider them to be multimimittance logic elements. The logic elements using one information parameter are more preferable in practice. They use, for example, only active resistance – R (R-element), capacitor immitance – C (C-element) or inductive immitance – L (L-element). Such logic elements are monomimittance elements. Absence of researches for their realization and estimation of parameters defines relevance of the presented work.

MAIN PART

It is known that logic level of a video pulse logic element is defined by a values’ range of voltage or currents. Except voltage and current, the condition of electric chain, action with alternative current, can be characterized by differential active R, capacitor and inductive XL = ωL resistance. Hence, logic states of the scheme can be characterized also by the spectrum of values of these parameters. For example, logic unit – «1» corresponds to the range of change R m > Rp, and logic zero – «0» corresponds to the range of change R o < Rm (monoimmittance logic R-element), where Rm – resistive border of logic level. Similarly: for capacitance: «1»; «0» (monoimmittance logic C-element); for inductive resistance: «1» ≡ X L0 > XLo; «0» ≡ X L0 (monoimmittance logic L-element). Considering the limited volume of the publication, at the given stage we will be limited to consideration only monoimmittance R-elements.

As the simplest logical monoimmittance R-element “NOT” properties of quarterwave transmission line segment can be used that implements "quarter wave transformer" (Fig. 1) [5].

Fig. 1 - "Quarter wave transformer" (a) that implements monoimmittance gate "NOT", and its transfer characteristic (b) Output impedance of the transmission line segment depends on the resistance Zm, connected at its input. Z o = Z d/Z i and (1) where Zd – characteristic impedance of the transmission line.
If \( Z_{0i}=R_{0i} \), then \( Z_{\text{out}} = R_{\text{out}} = Z_0^2/R_{\text{in}} \). Considering that \( Z_0 \) has a real fixed value, the transfer characteristic of the element has the form shown in Fig. 1b. The graph shows when \( R_{\text{in}}>Z_0 \), \( R_{\text{out}}<Z_0 \) and vice versa, which corresponds to the conditions of constructing logical monoimittance R-element "NOT".

One possible embodiment of the logic monoimittance R-element "AND" scheme is shown in Fig. 2. The output resistance of the circuit provided that the length of the transmission line connecting segments 1 \( \ll \lambda \), where \( \lambda \) - length of the electromagnetic wave in transmission line is equal to

Equation (2) describes the immittance transfer characteristic diagram showing \( R_{\text{in}1} \) and \( R_{\text{in}2} \) family of rectangular hyperbola, whose position can be adjusted by the value of resistor \( R_3 \).

Let’s restrict the logic level "0" with the range of variation of the input resistance \( (0+R_0) \) and the level "1" - with range \( (R_0^{(1)}+R_0^{(2)}) \). To ensure the supply of the scheme for noise immunity, set the upper limit of the zero logic level at the output with \( (R_0^{(1)}+R_0^{(2)}) \) conditions. The lower border of this level \( R_{\text{out}}<0 \). Resulting from the requirements of noise immunity, the border level logic "1" on the output of the circuit can be defined by the condition: \( (R_0^{(1)}<R_0^{(2)}) \), \( (R_0^{(1)}<R_0^{(2)}) \). Given the restrictions introduced, the field work monoimittance logical R-element "AND" determined by the shaded squares "0" and "1" to Fig. 2b.

Assuming that the input channels ILE are identical, i.e. \( Z_0 = Z_{0i} \), from (3) we find

\[
R_{\text{out}} = \frac{Z_0^2(R_0^{(1)}+R_0^{(2)})}{Z_0^2+R_0^{(1)}R_0^{(2)}}.
\]  

(4)

It follows from (4) that the transfer characteristic immittance ILE on the plain coordinates \( R_{\text{in}1} \) and \( R_{\text{in}2} \) is a straight line (3b) whose position can be adjusted by setting the values of the impedances \( Z_{\text{out}1} \) and \( Z_{\text{out}2} \) transmission line segments.

Let’s identify the possible range of variation of the input immittance corresponding to a logical "zero" and "one". As can be seen from Fig. 3b, if \( R_{\text{out}}=R_{\text{in}2} \), when the area where the conditions provided by the truth table, will be logical "0" output - area «I», and the logical «I» - area «II» respectively.

![Fig. 3 - The electrical scheme (a) and the immittance transfer characteristic (b) of monoimittance logical R-element "OR"](image)

To ensure the supply of the scheme for noise immunity, it is necessary to limit the range of the active input immittance under the conditions: \( R_{\text{out}1}^{(1)} > R_{\text{in}1}^{(1)} \), \( R_{\text{out}1}^{(2)} = R_{\text{in}1}^{(2)} \), \( R_{\text{out}2}^{(2)} > R_{\text{in}2}^{(2)} \), \( R_{\text{out}2}^{(1)} > R_{\text{in}2}^{(1)} \). These conditions can be achieved by choosing the values of the impedances \( Z_{\text{out}1} \) and \( Z_{\text{out}2} \).

**CONCLUSION**

The monoimittance logical R-elements, implementing logical functions "AND", "OR" and "NOT" were developed in this article. The electric scheme and immittance transfer characteristics are presented and recommendations for their use are suggested.


